[DOCUMENT NAME] Specification

[TITLE OF THE INVENTION] A SEMICONDUCTOR DEVICE

[WHAT IS CLAIMED IS]

1. A semiconductor device having a field effect transistor formed in a semiconductor layer provided on a insulating layer, comprising:

a body electrode electrically connected to a channel forming region of said field effect transistor; and

a back gate electrode provided below the insulating layer as opposed to the channel forming region of said field effect transistor.

2. A semiconductor device having a field effect transistor formed in a semiconductor layer provided on an insulating layer, comprising:

a body electrode electrically connected to a channel forming region of said field effect transistor; and

a back gate electrode provided below the insulating layer as opposed to the channel forming region of said field effect transistor, and

wherein said body electrode and said back gate electrode are respectively formed in a semiconductor region of conduction type opposite to a channel of said field effect transistor.

3. A semiconductor device having a semiconductor base in which a second semiconductor layer is formed on a first semiconductor layer with an insulating layer interposed therebetween, and a field effect transistor formed in the second semiconductor layer, comprising:

a body electrode formed in the second semiconductor layer and comprised of a semiconductor region electrically connected to a channel forming region of said field effect transistor; and

a back gate electrode formed in said first semiconductor layer and comprised of a semiconductor region brought into contact with the insulating layer, and

wherein said back gate electrode is provided as opposed to the channel forming region of said field effect transistor, and the semiconductor region corresponding to said body electrode and the semiconductor region corresponding to said back gate electrode are respectively formed in a conduction type opposite to a channel of said field effect transistor.

4. The semiconductor device according to any of claims 1 to 3, wherein a potential for controlling carriers of conduction type opposite to a channel formed in an upper portion of the channel forming region of said field effect transistor is applied to each of said body electrode and said back gate electrode.

5. The semiconductor device according to any of claims 1 to 3, wherein a potential for inducing an electrical charge of conduction type opposite to the channel formed in the upper portion of the channel forming region of said field effect transistor, in a lower portion of said semiconductor layer opposite to said back gate electrode is applied to each of said body electrode and said back gate electrode.

6. A semiconductor device having a first conduction type field effect transistor and a second conduction type field effect transistor formed in a semiconductor layer provided on an insulating film, comprising:

a first body electrode electrically connected to a channel forming region of said first conduction type field effect transistor;

a first back gate electrode provided below said insulating layer in an opposing relationship to the channel forming region of said first conduction type field effect transistor;

a second body electrode electrically connected to a channel forming region of said second conduction type field effect transistor; and

a second back gate electrode provided below said insulating layer as opposed to the channel forming region of said second conduction type field effect transistor.

7. A semiconductor device having a first conduction type field effect transistor and a second conduction type field effect transistor formed in a semiconductor layer provided on an insulating film, comprising:

a first body electrode electrically connected to a channel forming region of said first conduction type field effect transistor;

a first back gate electrode provided below said insulating layer in an opposing relationship to the channel forming region of said first conduction type field effect transistor;

a second body electrode electrically connected to a channel forming region of said second conduction type field effect transistor; and

a second back gate electrode provided below said insulating layer as opposed to the channel forming region of said second conduction type field effect transistor, and

wherein said first body electrode and said first back gate electrode are respectively formed in a semiconductor region of conduction type opposite to a channel of said first conduction type field effect transistor, and said second body electrode and said second back gate electrode are respectively formed in a semiconductor region of conduction type opposite to a channel of said second conduction type field effect

transistor.

8. A semiconductor device having a semiconductor base in which a second semiconductor layer is formed on a first semiconductor layer with an insulating layer interposed therebetween, and a first conduction type field effect transistor and a second conduction type field effect transistor both formed in the second semiconductor layer, comprising:

a first body electrode formed in the second semiconductor layer and comprised of a semiconductor region electrically connected to a channel forming region of said first conduction type field effect transistor;

a first back gate electrode formed in the first semiconductor layer and comprised of a semiconductor region brought into contact with the insulating layer;

a second body electrode formed in the second semiconductor layer and comprised of a semiconductor region electrically connected to a channel forming region of said second conduction type field effect transistor; and

a second back gate electrode formed in the first semiconductor layer and comprised of a semiconductor region brought into contact with the insulating layer, and

wherein said first back gate electrode is provided as opposed to the channel forming region of said first

conduction type field effect transistor, said second back gate electrode is provided as opposed to the channel forming region of said second conduction type field effect transistor, the semiconductor region used as said first body electrode and the semiconductor region used as said first back gate electrode are respectively formed in a conduction type opposite to a channel of said first conduction type field effect transistor, and the semiconductor region used as said second body electrode and the semiconductor region used as said second back gate electrode are respectively formed in a conduction type opposite to a channel of said second conduction type field effect transistor.

9. The semiconductor device according to claim 8, wherein the semiconductor region used as said first back gate electrode and the semiconductor region used as said second back gate electrode are respectively electrically separated from said second semiconductor layer.

10. The semiconductor device according to any of claims 6 to 9, wherein a potential for controlling carriers of conduction type opposite to a channel formed in an upper portion of the channel forming region of said first conduction type field effect transistor is applied to each of said first body electrode and said first back gate electrode, and a potential for controlling carriers

of conduction type opposite to a channel formed in an upper portion of the channel forming region of said second conduction type field effect transistor is applied to each of said body electrode and said back gate electrode.

11. The semiconductor device according to any of claims 6 to 9, wherein a potential for inducing an electrical charge of conduction type opposite to the channel formed in the upper portion of the channel forming region of said first conduction type field effect transistor, in a lower portion of said semiconductor layer opposite to said first back gate electrode is applied to each of said first body electrode and said fist back gate electrode, and a potential for inducing an electrical charge of conduction type opposite to the channel formed in the upper portion of the channel forming region of said second conduction type field effect transistor, in a lower portion of said semiconductor layer opposite to said second back gate electrode is applied to each of said second body electrode and said second back gate electrode.

12. A method of driving a semiconductor device having a field effect transistor formed in a semiconductor layer provided on an insulating layer, a body electrode electrically connected to a channel

forming region of said field effect transistor, and a back gate electrode provided below the insulating layer in an opposing relationship to the channel forming region of said filed effect transistor, comprising the following step of:

applying a potential lying in a direction to induce an electrical charge of conduction type opposite to a channel formed in a surface layer of the channel forming region of said field effect transistor, in a lower portion of the channel forming region thereof to said body electrode and said back gate electrode or at least said back gate electrode so as to increase a threshold voltage of said field effect transistor.

13. A method of driving a semiconductor device having a field effect transistor formed in a semiconductor layer provided on an insulating layer, a body electrode electrically connected to a channel forming region of said field effect transistor, and a back gate electrode provided below the insulating layer in an opposing relationship to the channel forming region of said filed effect transistor, comprising the following step of:

applying a potential lying in a direction to induce an electrical charge of conduction type opposite to a channel formed in a surface layer of the channel forming region of said field effect transistor, in a lower

portion of the channel forming region thereof to said body electrode and said back gate electrode or at least said back gate electrode so as to stabilize a threshold voltage of said field effect transistor and increase a withstand voltage of the drain thereof.

14. A method of driving a semiconductor device having a first conduction type field effect transistor and a second conduction type field effect transistor both formed in a semiconductor layer provided on an insulating layer, a first body electrode electrically connected to a channel forming region of said first conduction type field effect transistor, a first back gate electrode provided below the insulating layer as opposed to the channel forming region of said first conduction type field effect transistor, a second body electrode electrically connected to a channel forming region of said second conduction type field effect transistor, and a second back gate electrode provided below the insulating layer as opposed to the channel forming region of said second conduction type field effect transistor, comprising the following steps of:

in a first conduction type field effect transistor and a second conduction type field effect transistor constituting a predetermined circuit block, applying a potential lying in a direction to induce an electrical charge of conduction type opposite to a channel formed in

a surface layer of the channel forming region of said first conduction type field effect transistor, in a lower portion of the channel forming region thereof to said first body electrode and said first back gate electrode or at least said first back gate electrode so as to increase a threshold voltage of said first conduction type field effect transistor to thereby allow low power consumption, applying a potential lying in a direction to induce an electrical charge of conduction type opposite to a channel formed in a surface layer of the channel forming region of said second conduction type field effect transistor, in a lower portion of the channel forming region thereof to said second body electrode and said second back gate electrode or at least said second back gate electrode so as to increase a threshold voltage of said second conduction type field effect transistor to thereby allow low power consumption, and activating each of a first conduction type field effect transistor and a second conduction type field effect transistor constituting another circuit block at high speed in a state of being brought to a low threshold voltage.

15. A method of driving a semiconductor device having a first conduction type field effect transistor and a second conduction type field effect transistor both formed in a semiconductor layer provided on an insulating layer, a first body electrode electrically connected to a

channel forming region of said first conduction type field effect transistor, a first back gate electrode provided below the insulating layer as opposed to the channel forming region of said first conduction type field effect transistor, a second body electrode electrically connected to a channel forming region of said second conduction type field effect transistor, and a second back gate electrode provided below the insulating layer as opposed to the channel forming region of said second conduction type field effect transistor, comprising the following steps of:

changing with time, potentials applied to said first back gate electrode and said second back gate electrode, or said first back gate electrode, said second back gate electrode, said first body electrode and said second body electrode; and

thereby varying characteristics of said first conduction type field effect transistor and said second conduction type field effect transistor.

16. A method of testing a semiconductor device having a first conduction type field effect transistor and a second conduction type field effect transistor both formed in a semiconductor layer provided on an insulating layer, a first body electrode electrically connected to a channel forming region of said first conduction type field effect transistor, a first back gate electrode

provided below the insulating layer as cpposed to the channel forming region of said first ccnduction type field effect transistor, a second body electrode electrically connected to a channel forming region of said second conduction type field effect transistor, and a second back gate electrode provided below the insulating layer as opposed to the channel forming region of said second conduction type field effect transistor, comprising the following step of:

measuring a leak current in a state in which potentials are respectively applied to said first back gate electrode and said second back gate electrode, or said first back gate electrode, said second back gate electrode, said first body electrode and said second body electrode so as to increase threshold voltages of said first conduction type field effect transistor and said second field effect transistor.

17. A method of aging a semiconductor device having a field effect transistor formed in a semiconductor layer provided on an insulating layer, a body electrode electrically connected to a channel forming region of said field effect transistor, and a back gate electrode provided below the insulating layer as opposed to the channel forming region of said field effect transistor, comprising the following step of:

performing aging in a state in which a potential is

applied to said back gate electrode or said back gate electrode and said body electrode.

18. A method of using a semiconductor device having a field effect transistor formed in a semiconductor layer provided on an insulating layer and having a body electrode electrically connected to a channel forming region of said field effect transistor, and a back gate electrode provided below the insulating layer as opposed to the channel forming region of said field effect transistor, comprising the following steps of:

forming a channel of conduction type opposite to a channel formed in a surface layer of the channel forming region of said field effect transistor at a lower portion of the channel forming region thereof, based on a potential applied to said body electrode and a potential applied to said back gate electrode; and

using said semiconductor device in a state in which said former channel and part of a depletion layer of a drain region for said field effect transistor are terminated.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invnetion]

The present invention relates to a semiconductor device, and particularly to a technique effective for application to a semiconductor device having a field

effect transistor formed in a semiconductor layer provided on an insulating layer.

[0002]

[Prior Art]

An attempt to use a semiconductor base having a so-called SOI (Silicon On Insulator) structure provided with an insulating layer composed of silicon oxide between a semiconductor substrate composed of monocrystal silicon and a thin semiconductor layer composed of monocrystal silicon and form a field effect transistor in a semiconductor layer of the semiconductor base has been made in a semiconductor device having the field effect transistor. The field effect transistor has a channel forming region (body region), a gate insulator, a gate electrode and a pair of semiconductor regions corresponding to source and drain regions and is constructed with a structure wherein the bottoms of the pair of semiconductor regions corresponding to the source and drain regions are brought into an insulating layer of a semiconductor base. Since the field effect transistor can reduce pn junction capacities (parasitic capacities) added to the source and drain regions by portions equivalent to contact areas of the respective bottoms of the pair of semiconductor regions, a switching speed can be rendered fast.

[0003]

On the other hand, since the periphery of the

channel forming region is surrounded by the pair of semiconductor regions and the insulating layer of the semiconductor base, the above-described field effect transistor is reduced in threshold voltage (Vth) as compared with the case in which a field effect transistor is formed in a semiconductor base comprised of a normal bulk substrate. Therefore, a method of providing a feeding contact region (body electrode) electrically connected to a channel forming region within a semiconductor layer of a semiconductor base and applying a potential to the feeding contact region to thereby vary a threshold voltage has been proposed for a partial depletion type field effect transistor in which a channel forming region is not completely depleted and some thereof remains as a neutral region. This method has been disclosed in, for example, 1997 IEEE International Solid-State Circuit Conference, Digest of Technical Papers, 68-69 TP 4.3 [A 1V 46ns 16Mb SOI-DRAM with Body Control Technique].

[0004]

Further, a method of providing a back gate electrode below an insulating layer of a semiconductor base as opposed to a channel forming region and applying a potential to the back gate electrode to thereby change a threshold voltage has been proposed for a complete depletion type field effect transistor wherein the channel forming region is completely depleted. This

method has been disclosed in Japanese Patent Application Laid-Open No. Hei 7-131025.

[0005]

[Problems to be Solved by the Invention]

(1) When the partial depletion type field effect transistor is of, for example, an n channel conduction type, a p type channel forming region produces a depleted region due to a gate electric field and potentials applied to its source and drain, and some thereof serves as a neutral region. When a VGS potential is applied to a gate electrode, a VS potential (= 0 [V]) is applied to one semiconductor region, a VDS potential (≥ VS potential) is applied to the other semiconductor region, and a VSub potential (≤ 0 [V]) is applied to a feeding contact region, a channel current flows so that electrons and holes are developed in a high field region near the drain. The electrons flow into a drain region higher in potential, whereas the holes flow into a neural region low in potential. The holes are drawn or drained to the feeding contact region through the neutral region. Since, however, the resistance of the neutral region is high, the neutral region becomes high in potential. Since the electrons flow from the source to a channel according to a bipolar operation when the neutral region is high in potential, the occurrence of the holes increases in the high field region near the drain. A problem arises in that since the potential of the neutral region increases

more and more due to the circulation of these series of mechanisms, the withstand voltage for the drain becomes low consequently. A further problem arises in that the threshold voltage becomes unstable. These problems arise similarly even in the case of a p channel conduction type. [0006]

(2) When the complete depletion type field effect transistor is of, for example, an n channel conduction type, each channel forming region is completely depleted. Therefore, there is no escape route of holes produced in a high field region near its drain. Therefore, a problem arises in that since all the generated holes flow into a source region, the withstand voltage for the drain becomes low due to a bipolar operation. A further problem arises in that since the channel forming region is completely depleted, a threshold voltage cannot be increased. A method of changing the threshold of a complete depletion type field effect transistor by a back gate bias has been disclosed in Japanese Patent Application Laid-Open No. Hei 1(1989)-115394. Since, however, the potential of a lower portion (lower surface portion) of a channel forming region is lowered by a minus back gate potential as a result of its detailed discussions, holes generated in the vicinity of the drain are stored in a lower portion of a channel forming region and hence the threshold voltage becomes unstable. These problems arise similarly even in the case of a p channel

conduction type.

[0007]

(3) The partial depletion type field effect transistor and the complete depletion type field effect transistor are respectively low in threshold voltage and also low in drain withstand voltage as described above. Thus, since the threshold voltage cannot be changed in a stable state, a standby current becomes large and hence a standby current test cannot be carried out. Further, since the withstand voltage for the drain is low, high-voltage aging cannot be performed.

[0008]

An object of the present invention is to provide a technique capable of increasing a withstand voltage for a drain of a field effect transistor formed in a semiconductor layer provided on an insulating layer.

[0009]

Another object of the present invention is to provide a technique capable of achieving the stabilization of a threshold voltage of a field effect transistor formed in a semiconductor layer provided on an insulating layer.

[0010]

A further object of the present invention is to provided a technique capable of changing a threshold voltage of a field effect transistor formed in a semiconductor layer provided on an insulating layer in a

stable state.

The above, other objects and novel features of the present invention will become apparent from the description of the present specification and the accompanying drawings.

[0011]

[Means for Solving the Problems]

Summaries of typical ones of the inventions disclosed in the present application will be described in brief as follows:

A semiconductor device having a field effect transistor formed in a semiconductor layer provided on a insulating layer comprises a body electrode electrically connected to a channel forming region of the field effect transistor, and a back gate electrode provided below the insulating layer as opposed to the channel forming region of the field effect transistor.

[0012]

In the case of a partial depletion type field effect transistor, a potential for inducing an electrical charge of conduction type opposite to a channel formed in an upper portion of the channel forming region of the field effect transistor, in a lower portion of the semiconductor layer opposite to the back gate electrode is applied to each of the body electrode and the back gate electrode.

[0013]

In the case of a complete depletion type field effect transistor, a potential (negative potential in the case of n channel conduction type) for drawing or draining carriers of conduction type opposite to the channel formed in the upper portion of the channel forming region of the field effect transistor is applied to the body electrode, and a potential for inducing an electrical charge of conduction type opposite to the channel formed in the upper portion of the channel forming region of the field effect transistor, in a lower portion of the semiconductor layer opposite to the back gate electrode is applied to the back gate electrode.

[0014]

According to the above-described means, the following operation and effects can be obtained.

(1) In the case of a partial depletion type field effect transistor, a channel of conduction type opposite to a channel formed in an upper portion of a channel forming region thereof is formed at a lower portion (bottom) of the channel forming region. Since carriers (holes in the case of n channel conduction type and electrons in the case of p channel conduction type) generated in a high field region near a drain thereof flow into a body electrode through the channel formed in the lower portion of the channel forming region, an increase in potential in a neutral region of the channel forming region can be controlled. It is thus possible to

increase the withstand voltage for the drain of the partial depletion type field effect transistor. Further, the stabilization of a threshold voltage thereof can be achieved.

[0015]

Since the withstand voltage for the drain can be rendered high, high-voltage aging can be carried out.

[0016]

Further, since the withstand voltage for the drain can be increased and the stabilization of the threshold voltage can be achieved, the threshold voltage of the partial depletion type field effect transistor can be changed in a stable state.

[0017]

Furthermore, since the threshold voltage (Vth) of the partial depletion type field effect transistor can be varied in the stable state, a leak current test at standby can be carried out.

[0018]

(2) In the case of a complete depletion type field effect transistor, carriers (holes in the case of n channel conduction type and electrons in the case of p channel conduction type) generated in a high field region near a drain thereof are drained to a body electrode. Therefore, no carriers flow into a source region. Thus, since no bipolar operation is carried out, the withstand voltage for the drain of the complete depletion type

field effect transistor can be increased. Further, the stabilization of a threshold voltage thereof can be achieved.

[0019]

Since the withstand voltage for the drain can be set high, high-voltage aging can be carried out.

[0020]

Further, since the carriers of conduction type opposite to a channel formed in an upper portion of a channel forming region are drained by the body electrode, the threshold voltage of the complete depletion type field effect transistor can be changed in a stable state according to the potential of a back gate electrode.

[0021]

Furthermore, since the threshold voltage (Vth) of the complete depletion type field effect transistor can be changed in the stable state, a leak current test at standby can be carried out.

[0022]

Incidentally, when a potential for injecting an electrical charge of conduction type opposite to the channel formed in the upper portion of the channel forming region is applied to the body electrode in the complete depletion type field effect transistor, it assumes a partial depletion type without taking a complete depletion type. In this case, the threshold voltage can be changed according to the potential of the

body electrode as described in the partial depletion type field effect transistor.

[0023]

[MODE FOR CARRYING OUT THE INVENTION]

Embodiments of the present invention will hereinafter be described in detail with reference to the accompanying drawings.

(Embodiment 1)

In the present embodiment, an example in which the present invention is applied to a semiconductor device having a partial depletion type field effect transistor, will be explained.

Fig. 1 is a fragmentary plan view of a semiconductor device showing the embodiment 1 of the present invention. Figs. 2 and 3 are respectively fragmentary cross-sectional views of the semiconductor device referred to above. Fig. 2(A) and Fig. 3(A) are respectively cross-sectional views cut in a position taken along line A - A shown in Fig. 1. Fig. 2(B) and Fig. 3(B) are respectively cross-sectional views cut in a position taken along line B - B shown in Fig. 1. Incidentally, an illustration of each layer above a gate electrode 4 to be described later is omitted in Fig. 1 to make it easy to see the drawing. In Figs. 2 and 3, illustrations of layers above wires or interconnections (10A, 10B and 10C) to be described later are omitted to make it easy to see the drawings.

[0024]

As shown in Figs. 1 and 2, the semiconductor device is comprised principally of a semiconductor base 1. The semiconductor base 1 is comprised of a so-called SOI (Silicon On Insulator) structure wherein an insulating layer 1B composed of a silicon oxide film is provided between a p type semiconductor substrate 1A composed of monocrystal silicon and a semiconductor layer 1C composed of monocrystal silicon.

[0025]

A field insulating film 2 composed of, for example, a silicon oxide film is provided on element-to-element separation regions of the semiconductor layer 1C. A field effect transistor Qn is formed in an element forming region of the semiconductor layer 1C, whose periphery is defined by the field insulating film 2. In the present embodiment, the field effect transistor Qn is formed in a partial depletion type.

[0026]

Boron (B) is introduced into each region of the semiconductor layer 1C, in which the field effect transistor Qn is formed, and it is formed as a p type semiconductor region.

[0027]

The field effect transistor Qn principally comprises a channel forming region 1C comprised of a p type semiconductor layer 1C, a gate insulator 3, a gate

electrode 4, and a pair of n type semiconductor regions 6 which serve as source and drain regions respectively. Namely, the field effect transistor Qn is formed in an n channel conduction type. The gate insulator 3 is formed of, for example, a thermal oxidation silicon film. The gate electrode 4 is formed of a polycrystalline silicon film in which, for example, phosphorus (P) is introduced as an impurity. The pair of n type semiconductor regions 6 serving as the source and drain regions is formed in self-alignment with the gate electrode 4 and provided within the p type semiconductor layer 1C.

[0028]

The field effect transistor Qn is constructed in the form of a structure wherein the respective bottoms of the pair of n type semiconductor regions 6 corresponding to the source and drain regions are brought into contact with the insulating layer 1B of the semiconductor base 1. In the field effect transistor Qn, pn junction capacities (parasitic capacities) added to the source and drain regions can be respectively reduced by portions equivalent to the contact areas of the respective bottoms of the pair of n type semiconductor regions 6. It is therefore possible to make a switching speed fast.

[0029]

In the field effect transistor Qn, the periphery of the channel forming region thereof is surrounded by the pair of n type semiconductor regions 6 and the insulating

layer 1B of the semiconductor base 1.

[0030]

The p type semiconductor layer 1C is provided with a p type semiconductor region 8 used as a body electrode. The p type semiconductor region 8 is set to a high impurity concentration as compared with an impurity concentration of the p type semiconductor layer 1C and is electrically connected to the channel forming region of the field effect transistor Qn.

[0031]

A p type semiconductor region 5, which serves as a back gate electrode, is provided on a principal surface of the p type semiconductor substrate 1A. The p type semiconductor region 5 is set to a high impurity concentration as compared with an impurity concentration of the p type semiconductor substrate 1A and is provided so as to contact the insulating layer 1B. Further, the p type semiconductor region 5 is provided so as to be opposed to the p type semiconductor layer 1C in which the field effect transistor Qn is constituted. Namely, the p type semiconductor region 5 serving as the back gate electrode is provided so as to be opposed to each of the channel forming region of the field effect transistor Qn and the p type semiconductor region 8 used as the body electrode.

[0032]

The interconnection 10A is electrically connected

to one of the pair of n type semiconductor regions 6 through its corresponding connecting hole defined in an interlayer dielectric 9, whereas the interconnection 10B is electrically connected to the other of the n type semiconductor regions 6 through its corresponding connecting hole defined in the interlayer dielectric 9. A VS potential (= 0[V]) is applied to the interconnection 10A, and a VDS potential (≥ VS potential) is applied to the interconnection 10B. Namely, the VS potential is applied to one n type semiconductor region 6, whereas the VDS potential higher than the VS potential is applied to the other n type semiconductor region 6. Incidentally, a VGS potential is applied to the gate electrode 4.

[0033]

The interconnection 10C is electrically connected to the p type semiconductor region 8 used as the body electrode through its corresponding connecting hole defined in the interlayer dielectric 9. A VSub potential (≤ 0 [V]) lower than the VS potential and VDS potential is applied to the interconnection 10C. Namely, the VSub potential is applied to the p type semiconductor region 8 used as the body electrode.

[0034]

A VBG potential (< 0 [V]) lower than the VS potential and the VDS potential is applied to the p type semiconductor region 5 which serves as the back gate electrode. The VBG potential is supplied from the

principal surface side of the semiconductor base 1.

[0033]

In the semiconductor device, a depleted region 7A is developed in the channel forming region of the field effect transistor Qn owing to a gate electric field and source and drain potentials. Some of the depleted region 7A serves as a neutral region 7B. When the VGS potential is applied to the gate electrode 4, the VS potential (= 0 [V]) is applied to one n type semiconductor region 6, the VDS potential (≥ VS potential) is applied to the other n type semiconductor region 6, the VSub potential (≤ 0 [V]) is applied to the p type semiconductor region 8 used as the body electrode, and the VBG potential (< 0 [V]) is applied to the p type semiconductor region 5 used as the back gate electrode, a channel 11 of conduction type opposite to a channel formed in an upper portion of the channel forming region of the field effect transistor Qn is formed at a lower portion (bottom) of the p type semiconductor layer 1C opposite to the p type semiconductor region 5 used as the back gate electrode. Since the p type semiconductor region 5 used as the back gate electrode is provided in opposing relationship to each of the channel forming region of the field effect transistor Qn and the p type semiconductor region 8 used as the body electrode in the present embodiment, the channel forming region of the field effect transistor Qn and the p type semiconductor region 8 used as the body

electrode are kept in a state of being connected to each other through the channel 11. Since holes produced in a high field region lying in the vicinity of the drain flow into the p type semiconductor region 3 used as the body electrode through the channel 11 formed at the lower portion of the channel forming region, a rise in the potential of the neutral region 7B in the channel forming region can be controlled. Thus, the withstand voltage of the drain of the partial depletion type field effect transistor Qn can be rendered high. It is also possible to stabilize a threshold voltage (Vth).

[0036]

Since the drain withstand voltage can be set high, high-voltage aging can be carried out. The aging is done in a state in which the potential is applied to the back gate electrode or the back gate electrode and body electrode. The aging means a screening test for activating circuits in a semiconductor device under a use condition (in a load-applied state) severer than a use condition for each customer, generating one brought to defectiveness when being in use by the customer, in a given sense, a defect at an increasingly fast rate, and eliminating each defective in the initial stage prior to the shipment to the customer.

[0037]

Further, since the drain withstand voltage can be increased and the stabilization of the threshold voltage

(Vth) can be achieved, the threshold voltage (Vth) of the partial depletion type field effect transistor Qn can be changed in a stable state.

[0038]

Since the threshold voltage of the partial depletion type field effect transistor can be varied in the stable state, a leak current test at standby can be carried out. The leak current test is carried out in a state in which the potential has been applied to the back gate electrode or the back gate electrode and body electrode, in such a manner that the threshold voltage of the field effect transistor is increased.

[0039]

Further, the potential applied to the back gate electrode or the back gate electrode and body electrode can be changed with time so as to vary the characteristic of the field effect transistor Qn.

[0040]

Incidentally, while the n channel conduction type field effect transistor has been described in the present embodiment, the present invention can obtain a similar effect even in the case of a p channel type conduction type field effect transistor.

[0041]

(Embodiment 2)

In the present embodiment, an example in which the present invention is applied to a semiconductor device

having a complete depletion type field effect transistor, will be described.

Fig. 4 is a fragmentary plan view of the semiconductor device showing the embodiment of the present invention. Fig. 5 is a fragmentary cross-sectional view of the semiconductor device, wherein Fig. 5(A) is a cross-sectional view cut in a position taken along line C - C shown in Fig. 4, and Fig. 5(B) is a cross-sectional view cut in a position taken along line D - D shown in Fig. 4. Incidentally, an illustration of each layer above a gate electrode 4 to be described later is omitted in Fig. 4 to make it easy to see the drawing. In Fig. 5, illustrations of layers above wires or interconnections (10A, 10B and 10C) to be described later are omitted to make it easy to see the drawings.

[0042]

As shown in Figs. 4 and 5, the semiconductor device according to the present embodiment is substantially identical in structure to the aforementioned embodiment 1. The present embodiment is different from the aforementioned embodiment in that a field effect transistor Qn is constructed in a complete depletion type, and the thickness of a p type semiconductor layer 1C is thinner than that of the p type semiconductor layer 1C of the aforementioned embodiment 1. Further, a VBG potential (< 0 [V]) is applied to a p type semiconductor region 5 used as a back gate electrode, and a VSub potential (≥ 0

[V]) is applied to a p type semiconductor region 8 used as a body electrode.

[0043]

The field effect transistor Qn employed in the present embodiment is constructed in a complete depletion type. When a VSG potential (> Vth) is applied to a gate electrode 4, a VS potential (0 [V]) is applied to one n type semiconductor region 6, a VDS potential (≥ VS potential) is applied to the other n type semiconductor region 6, the VSub potential (≥ 0 [V]) is applied to the p type semiconductor region 8 used as the body electrode, and the VBG potential (≤ 0 [V]) is applied to the p type semiconductor region 5 used as the back gate electrode, holes developed in a high field region lying in the vicinity of a drain are drawn or drained to the body electrode. Therefore, no holes flow into a source region. Thus, since no bipolar operation is performed, the withstand voltage for the drain of the complete depletion type field effect transistor Qn can be increased. It is also possible to stabilize a threshold voltage thereof.

[0044]

Since the drain withstand voltage can be set high, high-voltage aging can be carried out. The aging is done in a state in which the potential is applied to the back gate electrode or the back gate electrode and body electrode.

[0045]

Since carriers of conduction type opposite to a channel formed in an upper portion of a channel forming region are drawn or drained by the body electrode, the threshold voltage (Vth) of the complete depletion type field effect transistor Qn can be varied in a stable state by the potential applied to the back gage electrode (p type semiconductor region 5).

[0046]

Since the threshold voltage of the partial depletion type field effect transistor can be changed in the stable state, a leak current test at standby can be carried out. The leak current test is carried out in a state in which the potential has been applied to the back gate electrode or the back gate electrode and body electrode, in such a manner that the threshold voltage of the field effect transistor is increased.

[0047]

Further, the potential applied to the back gate electrode or the back gate electrode and body electrode can be changed with time so as to vary the characteristic of the field effect transistor Qn.

[0048]

When a potential for injecting electrical charges of conduction type opposite to the channel formed in the upper portion of the channel forming region is applied to the body electrode (p type semiconductor region 8) in the complete depletion type field effect transistor Qn

emplcyed in the present embodiment, the field effect transistor results in a partial depletion type without assuming the complete depletion type. As described in the partial depletion type field effect transistor employed in the aforementioned embodiment 1 in this case, the threshold voltage (Vth) can be changed by the potential applied to the body electrode.

[0049]

Fig. 6 shows a result obtained by examining the dependence of potentials applied to the body electrode and back gate electrode employed in the complete depletion type field effect transistor Qn on a threshold voltage thereof. When a minus potential is applied to the p type semiconductor region 6 used as the body electrode, the threshold voltage can be changed up to a logical value of a threshold voltage based on the potential application to the back gate electrode. In Fig. 6, Lg = 0.15 [μm] indicates a gate length of the gate electrode 4, tox = 3.5 [nm] indicates the thickness of a gate insulator 3, tSi = 50 [nm] indicates the thickness of the p type semiconductor layer 1C, Na = 2E17 [atoms/cm^3] indicates an impurity concentration of the p type semiconductor layer 1C, and tbox = 100 [nm] indicates the thickness of an insulating layer 1B.

[0050]

Since a channel of conduction type opposite to the channel formed in the upper portion of the channel

forming region is formed at a lower portion (bottom) of the channel forming region when a potential at an inclined portion shown in Fig. 6 is applied to the back gate electrode and body electrode, a partial depletion type field effect transistor is obtained. Since the holes are drawn or drained or they are injected from the p type semiconductor region 8 until the potential applied to the lower portion of the channel forming region becomes equal to the potential applied to the p type semiconductor region 8 used as the body electrode, the potential of the channel forming region is stable and the threshold voltage is also stable.

[0051]

Incidentally, while the n channel conduction type field effect transistor has been described in the present embodiment, the present invention can obtain a similar effect even in the case of a p channel conduction type field effect transistor.

[0052]

(Embodiment 3)

In the present embodiment, an example in which the present invention is applied to a semiconductor device having a complete depletion type field effect transistor, will be explained.

Fig. 7 is a fragmentary plan view of the semiconductor device showing the embodiment of the present invention, Fig. 8 is a cross-sectional view cut

in a position taken along line E - E shown in Fig. 7, and Fig. 9 is a plan view showing layouts of respective semiconductor regions in Fig. 7, respectively. Incidentally, an illustration of each layer above each gate electrode 27 to be described later is omitted in Fig. 7 to make it easy to see the drawing. Further, an illustration of each layer above a wire or interconnection 33A to be described later is omitted in Fig. 8 to make it easy to see the drawing.

[0053]

As shown in Figs. 7 and 8, the semiconductor device is comprised principally of a semiconductor base 20. The semiconductor base 20 is comprised of a so-called SOI (Silicon On Insulator) structure wherein an insulating layer 20B composed of a silicon oxide film is provided between a p type semiconductor substrate 20A composed of monocrystal silicon and a semiconductor layer 20C composed of monocrystal silicon.

[0054]

A field insulating film 21 composed of, for example, a silicon oxide film is provided on element-to-element separation regions of the semiconductor layer 20C. An n channel conduction type field effect transistor Qn and a p channel conduction type field effect transistor Qp are formed in an element forming region of the semiconductor layer 20C, whose periphery is defined by the field insulating film 2. In the present embodiment, the n

channel conduction type field effect transistor Qn and the p channel conduction type field effect transistor Qp are respectively formed in a complete depletion type.

[0055]

The field effect transistor Qn is formed in a p type semiconductor region 25A provided within the semiconductor layer 20C. The field effect transistor Qn is comprised principally of a channel forming region comprised of the p type semiconductor region 25A, a gate insulator 22, a gate electrode 27, and a pair of n type semiconductor regions 28 which serve as source and drain regions respectively. The gate insulator 22 is formed of, for example, a thermal oxidation silicon film. The gate electrode 27 is formed of, for example, a polycrystalline silicon film 23 and a W/TiN film 26 provided on the polycrystalline silicon film 23. For example, phosphorus (P) is introduced into the polycrystalline silicon film 23 as an impurity for reducing a resistance value.

[0056]

The field effect transistor Qp is formed in an n type semiconductor region 25B provided within the semiconductor layer 20C. The field effect transistor Qp is comprised principally of a channel forming region comprised of the n type semiconductor region 25B, a gate insulator 22, a gate electrode 27, and a pair of p type semiconductor regions 30 which serve as source and drain regions respectively. The gate insulator 22 is formed of,

for example, a thermal oxidation silicon film. The gate electrode 27 is formed of, for example, a polycrystalline silicon film 23 and a W/TiN film 26 provided on the polycrystalline silicon film 23. For example, boron (B) is introduced into the polycrystalline silicon film 23 as an impurity for reducing a resistance value.

[0057]

The field effect transistor Qn is constructed in the form of a structure wherein the respective bottoms of the pair of n type semiconductor regions 28 corresponding to the source and drain regions are brought into contact with the insulating layer 20B of the semiconductor base 20. In the field effect transistor Qn, pn junction capacities (parasitic capacities) added to the source and drain regions can be respectively reduced by portions equivalent to the contact areas of the respective bottoms of the pair of n type semiconductor regions 28. It is therefore possible to make a switching speed fast.

[0058]

The periphery of the channel forming region of the field effect transistor Qn is surrounded by the pair of n type semiconductor regions 28 corresponding to the source and drain regions and the insulating layer 20B of the semiconductor base 20.

[0059]

The field effect transistor Qp is constructed in the form of a structure wherein the respective bottoms of

the pair of p type semiconductor regions 30 corresponding to the source and drain regions are brought into contact with the insulating layer 20B of the semiconductor base 20. In the field effect transistor Qp, pn junction capacities (parasitic capacities) added to the source and drain regions can be respectively reduced by portions equivalent to the contact areas of the respective bottoms of the pair of p type semiconductor regions 30. It is therefore possible to make a switching speed fast.

[0060]

The periphery of the channel forming region of the field effect transistor Qp is surrounded by the pair of p type semiconductor regions 30 corresponding to the source and drain regions and the insulating layer 20B of the semiconductor base 20.

[0061]

As shown in Figs. 7, 8 and 9, the p type semiconductor region 25A is provided with a p type semiconductor region 31 used as a body electrode. The p type semiconductor region 31 is set to a high impurity concentration as compared with an impurity concentration of the p type semiconductor region 25A and is electrically connected to its corresponding channel forming region of the field effect transistor Qn.

[0062]

The n type semiconductor region 25B is provided with an n type semiconductor region 29 used a body

electrode. The n type semiconductor region 29 is set to a high impurity concentration as compared with an impurity concentration of the n type semiconductor region 25B and is electrically connected to its corresponding channel forming region of the field effect transistor Qp.

[0063]

A p type semiconductor region 24A, which serves as a back gate electrode, is provided on a principal surface of the p type semiconductor substrate 20A. The p type semiconductor region 24A is set to a high impurity concentration as compared with an impurity concentration of the p type semiconductor substrate 20A and is provided so as to contact the insulating layer 20B. Further, the p type semiconductor region 24A is provided so as to be opposed to the p type semiconductor region 25A in which the field effect transistor Qn is formed. Namely, the p type semiconductor region 24A used as the back gate electrode is provided so as to be opposed to each of the channel forming region of the field effect transistor Qn and the p type semiconductor region 31 used as the body electrode.

[0064]

An n type semiconductor region 24B used as a back gate electrode is provided on the principal surface of the p type semiconductor substrate 20A. The n type semiconductor region 24B is set to a high impurity concentration as compared with an impurity concentration

of the p type semiconductor substrate 20A and is provided so as to make contact with the insulating layer 20B. Further, the n type semiconductor region 24B is provided so as to be opposed to the n type semiconductor region 25B in which the field effect transistor Qp is formed. Namely, the n type semiconductor region 24B used as the back gate electrode is provided so as to be opposed to each of the channel forming region of the field effect transistor Qp and the n type semiconductor region 29 used as the body electrode.

[0065]

The interconnection 33A is electrically connected to one of the pair of n type semiconductor regions 28 of the field effect transistor Qn through its corresponding connecting hole defined in an interlayer dielectric 32. An interconnection 33C is electrically connected to the other n type semiconductor region 28 through its corresponding connecting hole defined in the interlayer dielectric 32.

[0066]

An interconnection 33B is electrically connected to one of the pair of p type semiconductor regions 30 of the field effect transistor Qp through its corresponding connecting hole defined in the interlayer dielectric 32, whereas the interconnection 33C is electrically connected to the other p type semiconductor region 30 through its corresponding connecting hole defined in the interlayer

dielectric 32.

[0067]

The gate electrodes 27 of the field effect transistors Qn and Qp are electrically connected to each other. Namely, the semiconductor device is equipped with an inverter circuit comprised of the field effect transistors Qn and Qp.

[0068]

An interconnection 33D is electrically connected to the p type semiconductor region 31 used as the body electrode through its corresponding connecting hole defined in the interlayer dielectric 32. The interconnection 33D is electrically connected to the p type semiconductor region 24A used as the back gate electrode through its connecting hole defined from the interlayer dielectric 32 to the insulating layer 20B. Namely, the same potential is applied to the p type semiconductor region 31 used as the body electrode and the p type semiconductor region 24A used as the back gate electrode.

[0069]

An interconnection 33E is electrically connected to the n type semiconductor region 29 used as the body electrode through its corresponding connecting hole defined in the interlayer dielectric 32. The interconnection 33E is electrically connected to the n type semiconductor region 24B used as the back gate

electrode through its corresponding connecting hole defined from the interlayer dielectric 32 to the insulating layer 20B. Namely, the same potential is applied to each of the n type semiconductor region 29 used as the body electrode and the n type semiconductor region 24B used as the back gate electrode.

[0070]

A VS potential is applied to the interconnection 33A, a VSD potential (≥ VS potential) is applied to the interconnection 33B, a Vsubp potential (≤0 [V]) is applied to the interconnection 33D, a Vsubn potential (> Vsubp potential) is applied to the interconnection 33E, and an input signal is applied to the interconnection 33C. Incidentally, Vsubp potential ≤ VS potential, Vsubn potential ≥ VDS potential and Vsubp potential < Vsubn potential. Further, the n type semiconductor region 24B, the p type semiconductor region 24A and the p type semiconductor substrate 20A are held in a reverse-bias relationship.

[0071]

A method of manufacturing the semiconductor device will next be explained with reference to Figs. 10 through 12 (fragmentary cross-sectional views for describing the manufacturing method).

As shown in Fig. 10(A), a semiconductor base 20 having an SOI structure provided with an insulating layer 20B composed of a silicon oxide film between a p type

semiconductor substrate 20A composed of monocrystal silicon and a semiconductor layer 20C composed of monocrystal silicon is first prepared. The p type semiconductor substrate 20A is set to an impurity concentration of about 1.5E15 [atoms/cm^3]. The insulating layer 20B is set to a thickness of about 100 [nm]. The semiconductor layer 20C is set to a thickness of about 50 [nm] and is not doped with an impurity.

[0072]

Next, a field insulating film 21 composed of a silicon oxide film, which has a thickness of about 100 [nm], is formed on the entire surface of the semiconductor layer 20C by a CVD method and thereafter subjected to patterning to thereby define or open an element forming region and a body electrode forming region of the semiconductor layer 20C as shown in Fig. 10(B). The patterning of the field insulating film 21 is carried out with a photoresist film as a mask.

[0073]

Next, a thermal oxidation process is performed to form a gate insulator 22 composed of a thermal oxidation silicon film having a thickness of about 3.5 [nm] on the element forming region of the semiconductor layer 20C. The thermal oxidation process is carried out in an atmosphere of partial-pressure steam at 900 [°C].

[0074]

Next, as shown in Fig. 11(C), a polycrystalline

silicon film 23 having a thickness of about 100 [nm] is formed on the entire surface of the semiconductor base 20 including the upper part of the gate insulator 22 by the CVD method.

[0075]

Next, boron is selectively introduced into the polycrystalline silicon film 23 opposite to a p channel conduction type field effect transistor forming region of the semiconductor layer 20C as an impurity by ion implantation. Thereafter, phosphorous is selectively introduced into the polycrystalline silicon film 23 opposite to an n channel conduction type field effect transistor forming region of the semiconductor layer 20C as an impurity by ion implantation. The introduction of boron is carried out under the condition that the final introduced amount thereof is about 2E15 [atoms/cm^2] and the amount of energy at its introduction is about 7 [Kev]. The introduction of phosphorous is carried out under the condition that the final introduced amount thereof is about 2E15 [atoms/cm^2] and the amount of energy at its introduction is about 20 [Kev]. The introduction of boron is performed for the purpose of bringing the gate electrode of the p channel conduction type field effect transistor into a p type, whereas the introduction of phosphorous is carried out for the purpose of bringing the gate electrode of the n channel conduction type field effect transistor into an n type.

[0076]

Next, a CMP (Chemical Mechanical Polishing) method is used to remove the polycrystalline silicon film 23 provided on the field insulating film 21.

[0077]

Next, boron (B) is selectively introduced into the p type semiconductor substrate 20A opposite to the n channel conduction type field effect transistor forming region of the semiconductor layer 20C as the impurity by ion implantation to thereby form a p type semiconductor region 24A which serves as a back gate electrode. The introduction of boron is carried out under the condition that the final introduced amount thereof is about 5E12 [atoms/cm^2] and the amount of energy at its introduction is about 120 [Kev]. The introduction of boron is performed with a photoresist film as a mask.

[0078]

Next, phosphorous (P) is selectively introduced into the p type semiconductor substrate 20A opposite to the p channel conduction type field effect transistor forming region of the semiconductor layer 20C as the impurity by ion implantation to thereby form an n type semiconductor region 24B which serves as a back gate electrode. The introduction of phosphorous is performed under the condition that the final introduced amount thereof is about 5E12 [atoms/cm^2] and the amount of energy at its introduction is about 260 [Kev]. The introduction

of phosphorous is carried out with a photoresist film as a mask. Thus, back gate potentials can be respectively independently applied to the back gate electrode of the field effect transistor Qn and the back gate electrode of the field effect transistor Qp.

[0079]

Next, boron is selectively introduced into the n channel conduction type filed effect transistor forming region of the semiconductor layer 20C as the impurity by ion implantation to thereby form a p type semiconductor region 25A. The introduction of boron is carried out under the condition that the final introduced amount thereof is about 1.5E12 [atoms/cm^2] and the amount of energy at its introduction is about 40 [Kev]. The introduction of boron is performed with a photoresist film as a mask.

[0080]

Next, phosphorous is selectively introduced into the p channel conduction type field effect transistor forming region of the semiconductor layer 20C as the impurity by ion implantation to thereby form an n type semiconductor region 25B. The introduction of phosphorous is carried out under the condition that the final introduced amount thereof is about 1.5E12 [atoms/cm^2] and the amount of energy at its introduction is about 100 [Kev]. The introduction of phosphorous is carried out with a photoresist film as a mask. According to this

process, the impurity concentration of the semiconductor layer 20C in the n channel conduction type field effect transistor forming region and the impurity concentration of the semiconductor layer 20C in the p channel conduction type field effect transistor forming region are respectively brought to about 2.0E17 [atoms/cm^3]. Further, the thickness of the semiconductor layer 20C is 50 [nm]. Therefore, the field effect transistors Qn and Qp are respectively activated as a complete depletion type. A process up to now is shown in Fig. 11(D).

[0081]

Next, as shown in Fig. 12(E), a W/TiN film 26 is formed on the entire surface of the semiconductor base 20 including the upper part of the polycrystalline silicon film 23. The W/TiN film 26 is formed by forming a TiN film having about 10 [nm] by a reactive sputtering method and thereafter forming a W film having about 50 [nm] by a sputtering method. The W/TiN film 26 is formed to achieve a reduction in the resistance of each gate electrode.

[0082]

Next, the W/TiN film 26 and the polycrystalline silicon film 23 are respectively successively subjected to patterning to thereby form gate electrodes 27 on the n channel conduction type field effect transistor forming region and p channel conduction type field effect transistor forming region of the semiconductor layer 20C. This patterning is carried out with a photoresist film as

a mask.

[0083]

Next, phosphorous is selectively introduced into an n channel conduction type field effect transistor forming region of the p type semiconductor region 25A and a body electrode forming region of the n type semiconductor region 25B as the impurity by ion implantation to thereby form a pair of n type semiconductor regions 28 corresponding to source and drain regions and an n type semiconductor region 29 corresponding to a body electrode. The introduction of phosphorous is carried out under the condition that the final introduced amount thereof is about 1.5E15 [atoms/cm^2] and the amount of energy at its introduction is about 20 [Kev]. The introduction of phosphorous is performed with a photoresist film as a mask.

[0084]

Next, boron is selectively introduced into a p channel conduction type field effect transistor forming region of the n type semiconductor region 25B and a body electrode forming region of the p type semiconductor region 25A as the impurity by ion implantation to thereby form a pair of p type semiconductor regions 30 corresponding to source and drain regions and a p type semiconductor region 31 corresponding to a body electrode. The introduction of boron is carried out under the condition that the final introduced amount thereof is

about 1.5E15 [atoms/cm^2] and the amount of energy at its introduction is about 7 [Kev]. The introduction of phosphorous is performed with a photoresist film as a mask.

[0085]

Next, a heat treatment is effected for 10 [seconds] at 950 [°C] to activate the pair of n type semiconductor regions 28, the n type semiconductor region 29, the pair of p type semiconductor regions 30 and the p type semiconductor region 31. A process up to now is shown in Fig. 12(F).

[0086]

Next, an interlayer dielectric 32 is formed on the entire surface of the semiconductor base 20 and thereafter connecting holes are defined. Afterwards, wires or interconnections 33A, 33B, 33C, 33D and 33E are respectively formed, whereby the state illustrated in Fig. 8 is reached.

[0087]

Thus, the present embodiment is provided with the body electrode comprised of the p type semiconductor region 31 electrically connected to the channel forming region of the n channel conduction type field effect transistor Qn, the back gate electrode comprised of the p type semiconductor region 24A provided below the insulating layer 20B as opposed to the channel forming region of the n channel conduction type field effect

transistor Qn, the body electrode comprised of the n type semiconductor region 29 electrically connected to the channel forming region of the p channel conduction type field effect transistor Qp, and the back gate electrode comprised of the n type semiconductor region 24B provided below the insulating layer 20B as opposed to the channel forming region of the p channel conduction type field effect transistor Qp. Therefore, when a potential is applied to each of the body electrode and back gate electrode, the withstand voltages for the drains of the n channel conduction type field effect transistor Qn and the p channel conduction type field effect transistor Qp can be increased, and the stabilization of the respective threshold voltages (Vth) of the n channel conduction type field effect transistor Qn and the p channel conduction type field effect transistor Qp can be achieved.

[0088]

Further, since the withstand voltages for the drains of the n channel conduction type field effect transistor Qn and p channel conduction type field effect transistor Qp can be set high, high-voltage aging can be carried out. The aging is done in a state in which the potential is applied to the back gate electrode or the back gate electrode and body electrode.

[0089]

Since carriers of conduction type opposite to a channel formed in an upper portion of the channel forming

region are drained by the body electrode comprised of the p type semiconductor region 31, the threshold voltage (Vth) of the field effect transistor Qn can be varied in a stable state according to the potential applied to the back gate electrode comprised of the p type semiconductor region 24A. Further, since the carries of conduction type opposite to the channel formed in the upper portion of the channel forming region are drawn or drained by the body electrode comprised of the n type semiconductor region 29, the threshold voltage (Vth) of the field effect transistor Qp can be changed in a stable state according to the potential applied to the back gate electrode comprised of the n type semiconductor region 24B.

[0090]

Since the respective threshold voltages of the n channel conduction type field effect transistor Qn and p channel conduction type field effect transistor Qp can be changed in the stable state, a leak current test at standby can be carried out. Lowering the threshold voltages (Vth) of the n channel conduction type field effect transistor Qn and p channel conduction type field effect transistor Qp upon operation allows a high-speed operation. The leak current test is carried out in a state in which the potential has been applied to the back gate electrode or the back gate electrode and body electrode, in such a manner that the threshold voltage of

the field effect transistor is increased.

[0091]

Further, the potential applied to the back gate electrode or the back gate electrode and body electrode can be changed with time so as to vary the characteristics of the field effect transistor Qn and the field effect transistor Qp.

[0092]

As shown in Fig. 22 (timing chart), V_1 = Vsubn potential (> VDS potential) is applied to the body electrode and back gate electrode of pMOS (p channel conduction type field effect transistor Qp) and V_2 = Vsubp potential (< VS potential) is applied to the body electrode and back gate electrode of nMOS (n channel conduction type field effect transistor Qn) upon standby. Consequently, Vth (threshold voltages) of pMOS and nMOS can be rendered high and hence leak current can be reduced. Further, a normal operation can be carried out by making Vsubn potential = VDS potential and Vsubp potential = VS potential (0 [V] potential) upon operation.

[0093]

(Embodiment 4)

In the present embodiment, an example in which the present invention is applied to a semiconductor device having a complete depletion type field effect transistor, will be described.

Fig. 13 is a fragmentary plan view of the

semiconductor device showing the embodiment 4 of the present invention. Fig. 14 is a cross-sectional view cut in a position taken along line F - F shown in Fig. 13. Incidentally, an illustration of each layer above a gate electrode 47 to be described later is omitted in Fig. 13 to make it easy to see the drawing. Further, an illustration of each layer above an interconnection 57A to be described later is omitted in Fig. 14 to make it easy to see the drawing.

[0094]

As shown in Figs. 13 and 14, the semiconductor device according to the present embodiment has a p type semiconductor layer 41A and an n type semiconductor layer 41B insulated and separated from each other by an insulating layer 40B. Further, a complete depletion type n channel conduction type p field effect transistor Qn is formed in the p type semiconductor layer 41A, and a complete depletion type p channel conduction type field effect transistor Qp is formed in the n type semiconductor layer 41B. Further, the semiconductor device according to the present embodiment is constructed so that potentials can be respectively independently applied to a p type semiconductor region 55 used as a body electrode and a p type semiconductor region 42A used as a back gate electrode. Furthermore, the semiconductor device is constructed in such a manner that potentials can be respectively independently applied to an n type

semiconductor region 51 used as a body electrode and an n type semiconductor region 42B used as a back gage electrode.

[0095]

A method of manufacturing the semiconductor device will be explained below with reference to Figs. 15 through 19 (fragmentary cross-sectional views for describing the manufacturing method).

As shown in Fig. 15(A), a semiconductor base 20 having an SOI structure provided with an insulating layer 40B composed of a silicon oxide film between a p type semiconductor substrate 40A composed of monocrystal silicon and a semiconductor layer 40C composed of monocrystal silicon is first prepared. The p type semiconductor substrate 40A is set to an impurity concentration of about 1.3E15 [atoms/cm^3]. The insulating layer 40B is set to a thickness of about 100 [nm]. The semiconductor layer 40C is set to a thickness of about 50 [nm] and is not doped with an impurity.

[0096]

Next, a thermal oxidation silicon film having a thickness of about 10 [nm], is formed on the surface of the semiconductor layer 40C. Thereafter, a silicon nitride film having a thickness of about 30 [nm] is formed on the surface of the thermal oxidation silicon film and thereafter subjected to patterning to thereby form individually separated masks M on an n channel

conduction type field effect transistor forming region and a p channel conduction type field effect transistor forming region of the semiconductor layer 40C.

[0097]

Next, a thermal oxidation process is performed to oxidize portions of the semiconductor layer 40C exposed from the masks M, thereby forming a semiconductor layer 41A and a semiconductor layer 41B insulated and separated from each other. A process up to now is shown in Fig. 15(B).

[0098]

Next, a wet etching process using an aqueous solution of hydrofluoric acid is performed and thereafter a wet etching process using a hot phosphoric acid solution is effected to remove the masks M. Afterwards, boron (B) is selectively introduced into the semiconductor layer 41A as an impurity by ion implantation to thereby form a p type semiconductor layer 41A having an impurity concentration of about 2E17 [atoms/cm^3]. The introduction of boron is carried out under the condition that the final introduced amount thereof is about 1E12 [atoms/cm^2] and the amount of energy at its introduction is about 10 [Kev]. The introduction of boron is performed with a photoresist film as a mask.

[0099]

Next, boron is selectively introduced into a principal surface of the semiconductor substrate 40A

opposite to the p type semiconductor layer 41A as the impurity by ion implantation to thereby form a p type semiconductor region 42A used as a back gate electrode. The introduction of boron is carried out under the condition that the final introduced amount thereof is about 1E13 [atoms/cm^2] and the amount of energy at its introduction is about 100 [Kev]. The introduction of boron is performed with a photoresist film as a mask. [0100]

Next, phosphorous is selectively introduced into the semiconductor layer 41B as an impurity by ion implantation to thereby form an n type semiconductor layer 41B having an impurity concentration of about 2E17 [atoms/cm^3]. The introduction of phosphorous is performed under the condition that the final introduced amount thereof is about 1E12 [atoms/cm^2] and the amount of energy at its introduction is about 25 [Kev]. The introduction of phosphorous is done with a photoresist film as a mask [0101]

Next, phosphorous is selectively introduced into the principal surface of the semiconductor substrate 40A opposite to the n type semiconductor layer 41B as the impurity by ion implantation to thereby form an n type semiconductor region 42B used as a back gate electrode. The introduction of phosphorous is carried out under the condition that the final introduced amount thereof is about 1E13 [atoms/cm^2] and the amount of energy at its

introduction is about 240 [Kev]. The introduction of phosphorous is performed with a photoresist film as a mask. A process up to now is shown in Fig. 16(C).

[0102]

Next, as shown in Fig. 16(D), a field insulating film 43 composed of a silicon oxide film having a thickness of about 100 [nm] is formed on the entire surface of the semiconductor base 40 including the upper part of the p type semiconductor layer 41A and n type semiconductor layer 41B. Thereafter, the field insulating film 43 is subjected to patterning to thereby define or open an element forming region and a body electrode forming region of the p type semiconductor layer 41A and an element forming region, a body electrode forming region and a feeding region of the n type semiconductor layer 41B as shown in Fig. 17(E). The patterning of the filed insulating film 43 is carried out with a photoresist film as a mask.

[0103]

Next, a thermal oxidation process is performed to form a gate insulator 44 composed of a thermal oxidation silicon film having a thickness of about 3.5 [nm] on the element forming regions of the p type semiconductor layer 41A and n type semiconductor layer 41B. The thermal oxidation process is carried out in an atmosphere of partial-pressure steam at 900 [°C].

[0104]

Next, as shown in Fig. 17(F), a polycrystalline silicon film 45 having a thickness of about 100 [nm] is formed on the entire surface of the semiconductor base 40 including the upper part of the gate insulator 44 by a CVD method.

[0105]

Next, phosphorous is selectively introduced into the polycrystalline silicon film 45 opposite to the p type semiconductor layer 41A as the impurity by ion implantation. Thereafter, boron is selectively introduced into the polycrystalline silicon film 45 opposite to the n type semiconductor layer 41B as the impurity by ion implantation. The introduction of phosphorous is carried out under the condition that the final introduced amount thereof is about 1.5E15 [atoms/cm^2] and the amount of energy at its introduction is about 15 [Kev]. The introduction of boron is carried out under the condition that the final introduced amount thereof is about 1.5E15 [atoms/cm^2] and the amount of energy at its introduction is about 5 [Kev]. The introduction of phosphorous is performed for the purpose of bringing the gate electrode of the n channel conduction type field effect transistor into an n type, whereas the introduction of boron is carried out for the purpose of bringing the gate electrode of the p channel conduction type field effect transistor into a p type.

[0106]

Next, a CMP (Chemical Mechanical Polishing) method is used to remove the polycrystalline silicon film 45 provided on the field insulating film 43.

[0107]

Next, as shown in Fig. 18(G), a W/TiN film 46 is formed on the entire surface of the semiconductor base 40 including the upper part of the polycrystalline silicon film 45. The W/TiN film 46 is formed by forming a TiN film having about 10 [nm] by a reactive sputtering method and thereafter forming a W film having about 50 [nm] by a sputtering method. The W/TiN film 46 is formed to achieve a reduction in the resistance of each gate electrode.

[0108]

Next, the W/TiN film 46 and the polycrystalline silicon film 45 are respectively successively subjected to patterning to thereby form gate electrodes 47 on the element forming region of the p type semiconductor layer 41A and the element forming region of the n type semiconductor layer 41B as shown in Fig. 18(H). This patterning is carried out with a photoresist film as a mask.

[0109]

Next, a first connecting hole for exposing the surface of part of the p type semiconductor region 42A, and a second connecting hole for exposing the surface of part of the n type semiconductor region 42B are respectively defined.

[0110]

Next, a buffer insulating film composed of a silicon oxide film having a thickness of about 5 [nm] is formed on the entire surface of the semiconductor base 40 by the CVD method.

[0111]

Next, phosphorous is selectively introduced into the element forming region of the p type semiconductor layer 41A, the body electrode forming region of the n type semiconductor layer 41B and the n type semiconductor region 42B exposed from the second connecting hole as the impurity by ion implantation to thereby form a pair of n type semiconductor regions 50 corresponding to source and drain regions, an n type semiconductor region 51 corresponding to a body electrode, and an n type semiconductor region 52 corresponding to a contact region. The introduction of phosphorous is carried out under the condition that the final introduced amount thereof is about 1.5E15 [atoms/cm^2] and the amount of energy at its introduction is about 20 [Kev]. The introduction of phosphorous is performed with a photoresist film as a mask.

[0112]

Next, boron is selectively introduced into the element forming region of the n type semiconductor layer 41B, the body electrode forming region of the p type semiconductor layer 41A and the p type semiconductor

region 42A exposed from the first connecting hole as the impurity by ion implantation to thereby form a pair of p type semiconductor regions 53 corresponding to source and drain regions, a p type semiconductor region 54 corresponding to a body electrode, and a p type semiconductor region 55 corresponding to a contact region. The introduction of boron is carried out under the condition that the final introduced amount thereof is about 1.5E15 [atoms/cm^2] and the amount of energy at its introduction is about 5 [Kev]. The introduction of phosphorous is performed with a photoresist film as a mask. A process up to now is illustrated in Fig. 19(I).

[0113]

Next, an interlayer dielectric 56 is formed on the entire surface of the semiconductor base 40. Thereafter, connecting holes are defined as shown in Fig. 19(J). Afterwards, wires or interconnections 57A through 57H are formed. Consequently, the state shown in Fig. 14 is reached.

[0114]

In a manner similar to the aforementioned embodiment 3, the semiconductor device according to the present embodiment as described above is provided with the body electrode comprised of the p type semiconductor region 55 electrically connected to the channel forming region of the n channel conduction type field effect transistor Qn, the back gate electrode comprised of the p

type semiconductor region 42A provided below the insulating layer 40B as opposed to the channel forming region of the n channel conduction type field effect transistor Qn, the body electrode comprised of the n type semiconductor region 51 electrically connected to the channel forming region of the p channel conduction type field effect transistor Qp, and the back gate electrode comprised of the n type semiconductor region 42B provided below the insulating layer 40B as opposed to the channel forming region of the p channel conduction type field effect transistor Qp. Therefore, the semiconductor device can obtain an effect similar to that obtained by the aforementioned embodiment 3. Further, the potentials can be respectively independently applied to the body electrode and back gate electrode.

[0115]

As shown in Fig. 23 (timing chart), Vsubn potential = V_1 potential (> VDS potential) and Vsubp potential = V_2 potential (< VS potential) are applied in a manner similar to the embodiment 3, so that Vth (threshold voltages) of pMOS (p channel conduction type field effect transistor Qp) and nMOS (n channel conduction type field effect transistor Qn) can be rendered high and hence leak current can be reduced.

[0116]

(Embodiment 5)

In the present embodiment, an example in which the

present invention is applied to a semiconductor device having a complete depletion type field effect transistor, will be described.

Fig. 20 is a fragmentary cross-sectional view of the semiconductor device showing the embodiment 5 of the present invention.

As shown in Fig. 20, the semiconductor device according to the present embodiment is substantially identical in structure to the aforementioned embodiment 3. The present embodiment is different from the aforementioned embodiments in that a p type semiconductor region 24A used as a back gate electrode is electrically isolated from a p type semiconductor substrate 20A by an n type semiconductor region 34. The p type semiconductor region 24A is provided in a principal surface of the n type semiconductor region 34, and the n type semiconductor region 34 is provided in a principal surface of the p type semiconductor substrate 20A.

[0117]

Owing to the electrical separation of the p type semiconductor region 24A used as the back gate electrode from the p type semiconductor substrate 20A by the n type semiconductor region 34 in this way, a back gate potential of a specific circuit block can be changed to a back gate potential of another circuit block.

[0118]

Further, since the back gate potential of the

specific circuit block and the back gate potential of another circuit block can be changed to each other, an n channel conduction type field effect transistor and a p channel conduction type field effect transistor constituting the specific circuit block are respectively brought to a high threshold voltage to achieve their low power consumption. Further, an n channel conduction type field effect transistor and a p channel conduction type field effect transistor constituting another circuit block are respectively brought to a low threshold voltage so that they can be activated at high speed.

[0119]

(Embodiment 6)

Fig. 21 is a block diagram showing operation modes of a RISC processor (semiconductor device) illustrative of an embodiment 6 of the present invention. In Fig. 21, reference numeral 50 indicates a vector register, reference numeral 51 indicates a cache controller, reference numeral 52 indicates a cache unit, reference numeral 53 indicates an arithmetic unit, reference numeral 54 indicates an arithmetic controller, reference numeral 55 indicates a main memory, and reference numeral 56 indicates a secondary cache, respectively.

[0120]

As shown in Fig. 21, a field effect transistor of the vector register 50 unused in a normal operation mode (1) is brought to a high Vth (high threshold), based on a

back gate potential. Further, field effect transistors of the cache controller 51 and cache unit 52 unused in a vector compute mode are respectively brought to a high Vth (high threshold), based on a back gate potential, i.e., the unused portions are brought to the high Vth, whereby low power consumption of the RISC processor can be achieved.

[0121]

[Effects of the Invention]

Effects obtained by typical ones of the inventions disclosed in the present application will be described in brief as follows:

A withstand voltage for a drain of a field effect transistor formed in a semiconductor layer provided on an insulating layer can be increased.

The stabilization of a threshold voltage of a field effect transistor formed in a semiconductor layer provided on an insulating layer can be achieved.

A threshold voltage of a field effect transistor formed in a semiconductor layer provided on an insulating layer can be changed in a stable state.

High-voltage aging can be carried out in a semiconductor device having a field effect transistors formed in a semiconductor layer provided on an insulating layer.

A leak current test for each field effect transistor formed in a semiconductor layer provided on an

insulating layer can be carried out.

[BRIEF DESCRIPTION OF THE DRAWINGS]

Fig. 1 is a fragmentary plan view of a semiconductor device showing an embodiment 1 of the present invention.

Fig. 2 is a fragmentary section cross-sectional view of the semiconductor device.

Fig. 3 is a fragmentary section cross-sectional view of the semiconductor device.

Fig. 4 is a fragmentary plan view of a semiconductor device showing an embodiment 2 of the present invention.

Fig. 5 is a fragmentary cross-sectional view of the semiconductor device.

Fig. 6 is a view showing the relationship between potentials applied to a body electrode and a back gate electrode and a threshold voltage.

Fig. 7 is a fragmentary plan view of a semiconductor device showing an embodiment 3 of the present invention.

Fig. 8 is a fragmentary cross-sectional view cut in a position taken along line E - E shown in Fig. 7.

Fig. 9 is a fragmentary plan view showing layouts of respective semiconductor regions shown in Fig. 7.

Fig. 10 is a fragmentary cross-sectional view for describing a method of manufacturing the semiconductor device.

Fig. 11 is a fragmentary cross-sectional view for describing the method of manufacturing the semiconductor device.

Fig. 12 is a fragmentary cross-sectional view for describing the method of manufacturing the semiconductor device.

Fig. 13 is a fragmentary plan view of a semiconductor device showing an embodiment 4 of the present invention.

Fig. 14 is a fragmentary cross-sectional view cut in a position taken along line F - F shown in Fig. 13.

Fig. 15 is a fragmentary cross-sectional view for describing a method of manufacturing the semiconductor device.

Fig. 16 is a fragmentary cross-sectional view for describing the method of manufacturing the semiconductor device.

Fig. 17 is a fragmentary cross-sectional view for describing the method of manufacturing the semiconductor device.

Fig. 18 is a fragmentary cross-sectional view for describing the method of manufacturing the semiconductor device.

Fig. 19 is a fragmentary cross-sectional view for describing the method of manufacturing the semiconductor device.

Fig. 20 is a fragmentary plan view of a

semiconductor device showing an embodiment 5 of the present invention.

Fig. 21 is a block diagram showing operation modes of a RISC processor (semiconductor device) illustrative of an embodiment 6 of the present invention.

Fig. 22 is a timing chart.

Fig. 23 is a timing chart.

[REFERENCE NUMERALS]

1 semiconductor base

1A p type semiconductor substrate

1B insulating layer

1C semiconductor layer

2 field insulating film

3 gate insulator

4 gate electrode

5 p type semiconductor region

6 n type semiconductor region

7A depleted region

7B neutral region

8 p type semiconductor region

9 interlayer dielectric

10A, 10B, and 10C interconnections

11 channel

Qn n channel conduction type field effect transistor

Qp p channel conduction type field effect transistor